On page 21, line 10, replace "defined" with --define--.

IN THE CLAIMS

Please amend claims 15 and 34 as set forth below.

15. (Once Amended) A device for [mapping interlaced real time video images onto a surface of a computer generated object, each video image including two interlaced half-frames of pixels] generating mipmaps from video sources, comprising:

[a filter unit for generating prefiltered images of less detail] a first adder configured to receive texels arriving from a video source, the first adder further configured to add two texels belonging to neighboring screen lines and to a same column;

a first FIFO buffer coupled to an output of the first adder, the first FIFO buffer configured to store an output value of the first adder when the first adder receives two texels belonging to neighboring screen lines and an even column;

a second adder having a first input coupled to the output of the first adder, a second input coupled to an output of the first FIFO buffer, and an output, the second adder configured to add in a next clock cycle

the even column stored in the first FIFO buffer and an odd column from the first adder; and

D1 cont.

[means for accessing pixels of a previous interlaced half-frame to perform said filtering] a second FIFO buffer configured to store an output of the second adder.

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34. (Once Amended) A device for [mapping real time video images onto a surface of a computer generated object, each video image comprising more than one scan-line] generating mipmaps from video sources, comprising;

[a filter unit for generating prefiltered images of less detail] a first adder configured to receive texels arriving from a video source, the first adder further configured to add two texels belonging to neighboring screen lines and to a same column;

D2

a first FIFO buffer coupled to an output of the first adder, the first FIFO buffer configured to store an output value of the first adder when the first adder receives two texels belonging to neighboring screen lines and an even column;

a second adder having a first input coupled to the output of the first adder, a second input coupled to an

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output of the first FIFO buffer, and an output, the second adder configured to add in a next clock cycle the even column stored in the first FIFO buffer and an odd column from the first adder;

a second FIFO buffer configured to store an output of the second adder;

a register coupled to an input of the first adder and configured to store texels from even columns for one clock cycle; and

[means for accessing pixels of a previous scan-line to perform said filtering] a circuit coupled to the output of the second adder and configured to compute mipmaps for the next higher level of detail.

REMARKS

The specification is being amended to correct a minor typographical error. Accordingly, Applicants respectfully request that the above amendments to the specification be approved. Applicants submit that no new matter has been added by virtue of the above amendments to the specification.

Claims 15 and 34 are rejected under 35 U.S.C. Section 112, second paragraph, as allegedly being indefinite for